The Cisco 7000 Series Router

The Cisco 7000 series router represented the next step in the evolution of the AGS and the Cbus architecture. Other than the mechanical structure and outward appearance, the 7000 wasn't drastically different from its predecessor, the AGS+. The biggest architectural difference was the elimination of the Multibus and Multibus interface cards—only Cbus interface cards were supported on the 7000.

Some of the changes were mostly superficial. On the 7000, the AGS+ processor card was replaced by the *Route Processor* (RP) card and the Cbus Controller was replaced by the 7000's *Switch Processor* (SP) card, but the RP and SP retained the same CPUs as their AGS+ counterparts. Although there was no Multibus, per se, on the 7000, the switching processor on the SP still connected to the main processor on the RP via a 155-Mbps Multibus-like interface. These similarities allowed the IOS software and switching processor microcode to work on the 7000 without requiring a large number of changes.

The 7000 did introduce a new hardware feature not present on the AGS+: *hot-swappable interface cards*. The 7000 routers allowed Cbus interface cards (called *interface processors* on the 7000) to be removed and re-inserted while IOS was operational with minimal operational disruption to other interface processors. When IOS detected that a card was being removed or inserted, it momentarily stalled operations on the Cbus while the insertion/removal was underway. When the insertion/removal completed, IOS resumed operation of the Cbus and continued switching packets where it left off.

This new feature necessitated a change in the operation of the switching processor microcode. Whereas the composition of interfaces was fixed on the AGS+ while IOS was in operation, on the 7000 that composition could change on the fly. The original switching processor microcode on the AGS+ was designed to carve a static MEMD buffer allocation at initialization time. On the 7000, however, the microcode had to be changed to re-carve the buffer allocation each time a card was inserted or removed. This allowed the SP to keep the most efficient use of packet memory resources even if the interface composition changed.

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SP (Switch Processor) card
Switch Processor (SP) card